# STIC Search Report
EIC 2100

## STIC Database Tracking Number: 183726

**TO: Benjamin R Bruckart**
**Location: RND 4A68**
**Art Unit: 2155**
**Friday, March 31, 2006**

**Case Serial Number: 10/781108**

**From: Lucy Park**
**Location: EIC 2100**
**RND-4B11**
**Phone: 571-272-8667**

**lucy.park@uspto.gov**

## Search Notes

Dear Examiner Bruckart,

Here are the search results for your Fast & Focused search request on case number 10/781108. I flagged the results that looked most relevant, but please review all of the results. Please let me know if you have any questions about these or if you need any further information.

Lucy

# STIC EIC 2100 Search Request Form

183726

Today's Date: 3/31/06

**What date would you like to use to limit the search?**

Priority Date: 9/29/00 Other:

Name ~~3/31~~ Ben Bruckart

AU 2155 Examiner # 79964

Room # 4A68 Phone 571-272-3982

Serial # 10/781,108

**Format for Search Results (Circle One):**

PAPER DISK (EMAIL)

**Where have you searched so far?**

(USP) (US Publications) DWPI EPO JPO ACM IBM TDB

IEEE INSPEC SPI Other _____

**Is this a "Fast & Focused" Search Request? (Circle One)** (YES) NO

A "Fast & Focused" Search is completed in 2-3 hours (maximum). The search must be on a very specific topic and meet certain criteria. The criteria are posted in EIC2100 and on the EIC2100 NPL Web Page at http://ptoweb/patents/stic/stic-tc2100.htm.

What is the topic, novelty, motivation, utility, or other specific details defining the desired focus of this search? Please include the concepts, synonyms, keywords, acronyms, definitions, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract, background, brief summary, pertinent claims and any citations of relevant art you have found.

**Is this request for an APPEALS or SARS case? (Circle One) YES (NO)**

I need a device that acts as an intermediary between a host computer ~~Lost~~ and a remote console. The device is within a host computer or externally directly connected to it. The host computer is controlled by the device and the device holds bootable images in the devices RAM. See claims, I and II. We are debating architecture. The device emulates a floppy drive.

Best Art Found 5,887,164 which is opposite of clm 11.

STIC Searcher Lucy Park Phone 28667

Date picked up 3/31/06 Date Completed 3/31/06

sira Search and Information Resources Administration

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File 347:JAPIO Nov 1976-2005/Nov(Updated 060302)
         (c) 2006 JPO & JAPIO
File 350:Derwent WPIX 1963-2006/UD,UM &UP=200621
         (c) 2006  Thomson Derwent

Set     Items   Description
S1    1115872   HOST? ? OR COMPUTER? ? OR PC? ? OR CLIENT? ?
S2    6950182   DEVICE? ? OR APPARATUS OR SUBSYSTEM? ? OR INTERMEDIAR???
S3     369003   CARD? ? OR BUS OR BUSES OR BUSSES OR NIC
S4       1114   (VIRTUAL OR EMULAT???)(3N)(DISK? ? OR DISKETTE? ? OR DRIVE?
                 ?)
S5    1019574   S2:S4(3N)(WITHIN OR WITH()IN OR INSIDE OR INTERNAL?? OR EM-
                BED???? OR CONTAIN??? OR INCLUD??? OR COUPLE OR COUPLED OR CO-
                NNECT???)
S6       1990   BOOT????(3N)IMAG??? OR (PREBOOT OR PRE()BOOT)()EXECUT???()-
                ENVIRONMENT OR PXE OR BOOTSTRAP???? OR PREBOOT????
S7    1057805   RAM OR MEMORY OR MEMORIES
S8         35   S1 AND S5 AND S6 AND S7
S9         28   S8 NOT AD=20000925:20030925/PR
S10        24   S9 NOT AD=20030925:20060331/PR
S11     82536   S3:S4(3N)(WITHIN OR WITH()IN OR INSIDE OR INTERNAL?? OR EM-
                BED???? OR CONTAIN??? OR INCLUD??? OR COUPLE OR COUPLED OR CO-
                NNECT???)
S12        15   S11 AND S1 AND S6
S13         4   S12 NOT S8
S14        61   S3:S4 AND S1 AND S6
S15        33   S14 AND S7
S16        18   S15 NOT (S8 OR S13)
S17        11   S16 NOT AD=20000925:20030925/PR
S18         8   S17 NOT AD=20030925:20060331/PR
S19       105   S3:S4 AND S6
S20        52   S19 AND (PROCESSOR? ? OR CPU OR MICROPROCESSOR? ? OR CHIP?
                 ?)
S21        37   S20 AND S7
S22        14   S21 NOT (S8 OR S13 OR S16)
S23        14   S22 NOT AD=20000925:20030925/PR
S24        13   S23 NOT AD=20030925:20060331/PR
S25         2   S3 AND S4 AND S6
S26      1118   (VIRTUAL OR EMULAT???)(3N)(DISK? ? OR DISKETTE? ? OR DRIVE?
                 ? OR FLOPPY)
S27        12   S26 AND S6
S28        10   S27 NOT (S8 OR S13 OR S16 OR S22 OR S25)
S29         5   S28 NOT AD=20000925:20030925/PR
S30         3   S29 NOT AD=20030925:20060331/PR
? logoff hold
       31mar06 10:56:03 User259273 Session D366.6
```

**10/5/17 (Item 15 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


009488542 **Image available**
WPI Acc No: 1993-182077/199322
Related WPI Acc No: 1992-034362
XRPX Acc No: N93-140028

**System utilities accessing appts for personal** computer **system - has processor,** ram **, rom and at least one direct access storage device storing utilities in same region as bios**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC )
Inventor: ARNOLD L R; BEALKOWSKI R; BLACKLEDGE J W; CRONK D S; DAYAN R A; GEISLER D R; MITTELSTEDT M T; PALKA M S; PAUL J D; SACHSENMAIER R; SMELTZER K D; WOYTOVECH P A; ZYVOLOSKI K M
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 5214695 | A | 19930525 | US 90557334 | A | 19900723 | 199322 | B |
| | | | US 91716594 | A | 19910617 | | |

Priority Applications (No Type Date): US 91716594 A 19910617; US 90557334 A 19900723
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 5214695 | A | | 30 | H04L-009/00 | CIP of application US 90557334<br>CIP of patent US 5128995 |

Abstract (Basic): US 5214695 A

A direct access storage **device** controller **coupled** between the system processor and direct access storage **device includes** a protection mechanism for protecting a region of the storage device. The protected region of the storage **device includes** a master **boot** record, a BIOS **image** and a system reference diskette image. The BIOS image includes a section known as Power on Self Test (POST).

POST is used to test and initialise a system. Upon detecting any configuration error, system utilities from the system reference diskette image, such as set configuration programs, diagnostic programs and utility programs can be automatically activated from the direct access storage device.

USE - Storing of system utilities is protected partition.

Dwg.2/13

Title Terms: SYSTEM; UTILISE; ACCESS; APPARATUS; PERSON; **COMPUTER** ; SYSTEM ; PROCESSOR; **RAM** ; ROM; ONE; DIRECT; ACCESS; STORAGE; DEVICE; STORAGE; UTILISE; REGION
Derwent Class: T01; T03
International Patent Class (Main): H04L-009/00
File Segment: EPI

DMA

10/5/22 (Item 20 from file: 350)
DIALOG(R)File 350:Derwent WPIX


003955672
WPI Acc No: 1984-101216/198416
XRPX Acc No: N84-075385

**Direct** memory **access interface arrangement - is for data communication channel to transfer data between** host **processor and remote data centre and eliminates ROM with** bootstrap **program**

Patent Assignee: AT & T BELL LAB (AMTT ); WESTERN ELECTRIC CO INC (AMTT )
Inventor: PETERSON T A
Number of Countries: 012 Number of Patents: 009
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| WO 8401449 | A | 19840412 | WO 83US1364 | A | 19830909 | 198416 | B |
| GB 2128000 | A | 19840418 | GB 8325793 | A | 19830927 | 198416 | |
| EP 120889 | A | 19841010 | EP 83903057 | A | 19830909 | 198441 | |
| JP 59501762 | W | 19841018 | JP 83503053 | A | 19830909 | 198448 | |
| US 4538224 | A | 19850827 | US 82428681 | A | 19820930 | 198537 | |
| CA 1194608 | A | 19851001 | | | | 198544 | |
| GB 2128000 | B | 19860910 | | | | 198637 | |
| EP 120889 | B | 19871216 | | | | 198750 | |
| DE 3374965 | G | 19880128 | | | | 198805 | |

Priority Applications (No Type Date): US 82428681 A 19820930
Cited Patents: 1.Jnl.Ref; EP 21489; EP 50434; JP 57143629; US 4093981; US 4075691
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| WO 8401449 | A | E | 33 | | |
| Designated States (National): JP | | | | | |
| Designated States (Regional): AT BE CH DE FR GB LU NL SE | | | | | |
| EP 120889 | A | E | | | |
| Designated States (Regional): DE FR NL | | | | | |
| EP 120889 | B | E | | | |
| Designated States (Regional): DE FR NL | | | | | |

Abstract (Basic): WO 8401449 A

The interface includes a buffer arrangement for storing data to be transferred between the **host** processor and the **memory** . A controller is **connected** to a data **bus** interconnecting the buffer arrangement, the peripheral processor and the **memory** . It is also **connected** to an address **bus** interconnecting the peripheral processor and the **memory** . The controller comprises a transfer arrangement responsive to control signals from the **host** processor to transfer information from the data bus to the address bus.

The controller is responsive to addresses on the address bus to store information appearing on the data bus. An initial **memory** address and program word count may be supplied to the interface arrangement and a peripheral processor program consisting of several program words which may be transferred to the program portion of the peripheral unit **memory** . A status register, responsive to control signals from the **host** processor, selectively regulates the controller and the transfer arrangement and inhibits operation of the peripheral processor. (33pp Dwg.No.1/10)

EP 120889 A

An interface unit (103) for loading therein a peripheral unit program received from a **host** processor, the interface unit comprising: a peripheral unit controller (213); and a peripheral unit (212); said peripheral unit having a random access **memory** (207); a

peripheral unit processor (208); a data bus (251) and an address bus (252) interconnecting said random access **memory** (207), said peripheral unit processor (208), and said peripheral unit controller (213); said random access **memory** having a data portion addressable with a data portion addressable with a data address for storing data and a program portion addressable with a program address for storing said program; said peripheral unit processor (208) being responsive to said program for transferring data between said **host** processor (101) and said data portion of said random access **memory** on said data bus; characterised in that said peripheral unit controller (213) comprises input buffer means (203) for transferring information including a controller address, said program address, and said program received from said **host** processor (101) onto said data bus (251); and an interface controller means (205) having **host** acess buffer means (801) for transferring said controller address received from said **host** processor on said data bus to said address bus (252), and responsive to said controller address on said address bus (252) and said program address received from said **host** processor (101) on said data bus (251) for addressing said program portion of said random access **memory** to load said program received from said **host** processor on said data bus into said program portion of said random access **memory** by direct **memory** access.

(18pp)

Title Terms: DIRECT; **MEMORY** ; ACCESS; INTERFACE; ARRANGE; DATA; COMMUNICATE; CHANNEL; TRANSFER; DATA; **HOST** ; PROCESSOR; REMOTE; DATA; CENTRE; ELIMINATE; ROM; **BOOTSTRAP** ; PROGRAM

Derwent Class: T01

International Patent Class (Additional): G06F-003/04; G06F-009/24; G06F-013/06

File Segment: EPI

**18/5/5 (Item 2 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


014065267 **Image available**
WPI Acc No: 2001-549480/200161
XRPX Acc No: N01-408171
Boot **code** image **creating method for-microprocessor based** computers , **involves copying stored** boot **code** image **to flash** memory card **in response to failing boot code creation bypass test**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC )
Inventor: AGUILAR M; GUPTA S; STAFFORD J M
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 6289449 | B1 | 20010911 | US 98211368 | A | 19981214 | 200161 | B |

Priority Applications (No Type Date): US 98211368 A 19981214
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 6289449 | B1 | | 17 | G06F-009/445 | |

Abstract (Basic): US 6289449 B1
NOVELTY - A **computer** is configured to fail a boot code creation bypass test. The bypass test is executed in response to a **boot** event. An **image** of **boot** code stored in a flash **memory** of the **computer** , is copied to a flash **memory card** , in response to failing the bypass test.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(a) **Computer** readable medium storing instructions for executing boot code creation bypass test;
(b) **Computer** network restoring method
USE - For microprocessor-based **computers** such as network **computers** and limited resource **computers** .
ADVANTAGE - The risk of corrupting and deleting the **computer** 's boot code is minimized by copying the **boot** code **image** from the flash **memory card** .
DESCRIPTION OF DRAWING(S) - The figure shows the flow diagram of **boot** code **image** creating method.
pp; 17 DwgNo 5/19
Title Terms: BOOT; CODE; IMAGE; METHOD; MICROPROCESSOR; BASED; **COMPUTER** ; COPY; STORAGE; BOOT; CODE; IMAGE; FLASH; **MEMORY** ; **CARD** ; RESPOND; FAIL; BOOT; CODE; CREATION; TEST
Derwent Class: T01
International Patent Class (Main): G06F-009/445
File Segment: EPI

**18/5/8 (Item 5 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


009783071
WPI Acc No: 1994-062924/199408
**High loading interface unit for GPIB connected to** host computer - **includes CPU having** bootstrap **program,** memory **for storing down loading program and for acting as buffer** memory **when down loading is executed, GPIB controller and inter-processor communication** bus **interface unit NoAbstract**
Patent Assignee: KOREA ELEC & TELECOM RES INST (KOEL-N)
Inventor: KIM J; YOON B
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| KR 9307082 | B | 19930729 | KR 8919573 | A | 19891227 | 199408 | B |

Priority Applications (No Type Date): KR 8919573 A 19891227
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| KR 9307082 | B | | | G06F-015/16 | |

Title Terms: HIGH; LOAD; INTERFACE; UNIT; GPIB; CONNECT; **HOST** ; **COMPUTER** ; CPU; **BOOTSTRAP** ; PROGRAM; **MEMORY** ; STORAGE; DOWN; LOAD; PROGRAM; ACT; BUFFER; **MEMORY** ; DOWN; LOAD; EXECUTE; GPIB; CONTROL; INTER; PROCESSOR; COMMUNICATE; **BUS** ; INTERFACE; UNIT; NOABSTRACT
Derwent Class: T01; W01
International Patent Class (Main): G06F-015/16
File Segment: EPI

**24/5/3 (Item 1 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


012993338 **Image available**
WPI Acc No: 2000-165190/200015
XRPX Acc No: N00-123688
Boot **control procedure for** image **forming apparatus e.g. fax machine - involves activating two IC** card **programs by switching write protection signal to highest order address of IC** card **, so that** CPU **boot process switches from internal flash** memory **to external IC** card memory
Patent Assignee: RICOH KK (RICO )
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| JP 2000020290 | A | 20000121 | JP 98202773 | A | 1998070 | 200015 | B |

Priority Applications (No Type Date): JP 98202773 A 19980702
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| JP 2000020290 | A | | 4 | G06F-009/06 | |

Abstract (Basic): JP 2000020290 A
NOVELTY - An IC **card** (11) sends a sleep signal to the **CPU** . Upon receiving the sleep signal, **CPU** switches the boot process from internal flash **memory** to IC **card** **memory** . Two kinds of programs from the IC **card** can be executed by switching the write protection (WP) signal to the highest order address of the IC.
USE - For controlling the **boot** procedure of an **image** forming apparatus.
ADVANTAGE - Offers cost reduction since two programs can be started from a general purpose IC **card** . DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of image forming apparatus control component. (11) IC **card** .
Dwg.1/2
Title Terms: BOOT; CONTROL; PROCEDURE; IMAGE; FORMING; APPARATUS; FACSIMILE ; MACHINE; ACTIVATE; TWO; IC; **CARD** ; PROGRAM; SWITCH; WRITING; PROTECT; SIGNAL; HIGH; ORDER; ADDRESS; IC; **CARD** ; SO; **CPU** ; BOOT; PROCESS; SWITCH; INTERNAL; FLASH; **MEMORY** ; EXTERNAL; IC; **CARD** ; **MEMORY**
Derwent Class: P75; T01; W02
International Patent Class (Main): G06F-009/06
International Patent Class (Additional): B41J-029/38; H04N-001/00
File Segment: EPI; EngPI

**24/5/4 (Item 2 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


012456350 **Image available**
WPI Acc No: 1999-262458/199922
XRPX Acc No: N99-195339
Bootstrap **mode testing and debugging of integrated circuits - configuring onchip microcontroller or digital signal** processor **to accept opcodes via external address and data pins, in test mode.**
Patent Assignee: ANONYMOUS (ANON )
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| RD 420018 | A | 19990410 | RD 99420018 | A | 19990320 | 199922 | B |

Priority Applications (No Type Date): RD 99420018 A 19990320
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| RD 420018 | A | | 2 | G06F-000/00 | |

Abstract (Basic): RD 420018 A
The method involves using the system reset to latch the group value of specific functional pins. The value is decoded to set the **chip** in the **bootstrap** mode, in which the external **memory** interface disables the internal boot ROM, and configures itself to allow a first access of the digital signal **processor** (DSP), or microcontroller, through an external address and data **bus** .
The asynchronous resetting is synchronised using the system clock and two phase latches to introduce a one cycle delay, and avoid recovery errors. If the decoded value of the group is 0000, the **bootstrap** signal is asserted.
USE - For systems on **chip** and DSP based **chips** , to configure test modes to ease simulation.
ADVANTAGE - Uses illegal code combination of existing functional pins to enter **bootstrap** mode, and does not waste simulation cycles or functional pins for test mode.
Dwg.1,2/2
Title Terms: **BOOTSTRAP** ; MODE; TEST; DEBUG; INTEGRATE; CIRCUIT; DIGITAL; SIGNAL; **PROCESSOR** ; ACCEPT; EXTERNAL; ADDRESS; DATA; PIN; TEST; MODE
Derwent Class: T01; U21
International Patent Class (Main): G06F-000/00
File Segment: EPI

**24/5/8 (Item 6 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


008701388
WPI Acc No: 1991-205408/199128
XRPX Acc No: N91-156826
Memory card **for** bootstrapping **operation in printer - is inserted in** processor **and has addresses reconfigured to boot from** card **which then allows flash EPROM to be programmed**
Patent Assignee: ANONYMOUS (ANON )
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| RD 326056 | A | 19910610 | | | | 199128 | B |

Priority Applications (No Type Date): RD 91326056 A 19910520

Abstract (Basic): RD 326056 A
A raster image **processor** is provided with flash EPROM to hold the basic operating program for the **processor** . A specially prepared **memory** board can be plugged into the **processor** and by controlling a normally unused pin on the serial port the addressing is altered to place the **memory card** at the **bootstrap** location.
Once the **processor** is run up from this **card** , the **processor** can run from **RAM** while reprogramming its own flash EPROM. Power for the reprogramming can be supplied through another unused pin.
ADVANTAGE - Allows for initial and subsequent reprogramming not requiring in-built ROMs or additional connectors. (Dwg. not available)
Title Terms: **MEMORY** ; **CARD** ; **BOOTSTRAP** ; OPERATE; PRINT; INSERT; **PROCESSOR** ; ADDRESS; RECONFIGURE; BOOT; **CARD** ; ALLOW; FLASH; EPROM; PROGRAM
Derwent Class: T01
International Patent Class (Additional): G06F-000/01
File Segment: EPI

**24/5/10 (Item 8 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


007572741 **Image available**
WPI Acc No: 1988-206673/198830
XRPX Acc No: N88-157579
**Mfg. smart** card **including** bootstrap **program - having electrically-erasable read only** memory **for storage of applications program subsequent to manufacture of** card
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC ); IBM CORP (IBMC )
Inventor: ABRAHAM D G; DOUBLE G P; NECKYFAROW S W; ROHLAND W S; TUNG M G; TUNG M H G
Number of Countries: 005 Number of Patents: 004
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| EP 275510 | A | 19880727 | EP 87118815 | A | 19871218 | 198830 | B |
| CN 8708157 | A | 19880831 | | | | 198933 | |
| EP 275510 | B1 | 19921021 | EP 87118815 | A | 19871218 | 199243 | |
| DE 3782328 | G | 19921126 | DE 3782328 | A | 19871218 | 199249 | |
| | | | EP 87118815 | A | 19871218 | | |

Priority Applications (No Type Date): US 874501 A 19870120
Cited Patents: A3...8914; No-SR.Pub; US 4613937; WO 8705420; EP 217281
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| EP 275510 | A | E | 9 | | |
| | Designated States (Regional): DE FR GB IT | | | | |
| EP 275510 | B1 | E | 10 | G07F-007/10 | |
| | Designated States (Regional): DE FR GB IT | | | | |
| DE 3782328 | G | | | G07F-007/10 | Based on patent EP 275510 |

Abstract (Basic): EP 275510 A
The **card** (10) has an instruction **processor** (12), read-only **memory** (14) and the electrically-eraseable read-only **memory** (16). Internal communications are effected on lines (20) and further input-output lines (18) connect the **card** to external devices.
The read-only **memory** (14) stores a **bootstrap** program which is loaded during manufacture of the **card** and provides the basic instruction repertoire and instructions for loading the applications program into the EEPROM (16). A flag (22) is set to indicate whether the applications program has been loaded or not.
ADVANTAGE - Program of **card** may be reloaded or changed as desired.
1/2
Title Terms: MANUFACTURE; SMART; **CARD** ; **BOOTSTRAP** ; PROGRAM; ELECTRIC; ERASE; READ; **MEMORY** ; STORAGE; APPLY; PROGRAM; SUBSEQUENT; MANUFACTURE; **CARD**
Derwent Class: T04
International Patent Class (Main): G07F-007/10
International Patent Class (Additional): G06F-009/02
File Segment: EPI

**24/5/12 (Item 10 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


004527462
WPI Acc No: 1986-030806/198605
XRPX Acc No: N86-022242
Microprocessor **based program store with** bootstrap **program - has program instructions stored in EPROM in several overlays individually selected by** bootstrap
Patent Assignee: RACAL DATACOM INC (RACA )
Inventor: CHENG J K; KAO M L
Number of Countries: 003 Number of Patents: 004
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| GB 2162346 | A | 19860129 | GB 8512329 | A | 19850515 | 198605 | B |
| US 4720812 | A | 19880119 | US 84615362 | A | 19840530 | 198805 | |
| CA 1235227 | A | 19880412 | | | | 198819 | |
| GB 2162346 | B | 19881116 | | | | 198846 | |

Priority Applications (No Type Date): US 84615362 A 19840530
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| GB 2162346 | A | | 10 | | |

Abstract (Basic): GB 2162346 B

The system is provided with a non-volatile store (58) (such as a PROM) which stores a **bootstrap** program, a non-volatile store (62) (such as an EPROM) which stores one or more program overlays, and a programmable volatile store (56) (such as a **RAM** ) which can be written into and read from. When the system is powered up, a **microprocessor** (50) executes the **bootstrap** program out of the PROM, which program includes instructions which copy the program instructions stored in the EPROM into the **RAM** .

The **microprocessor** then executes the program instructions out of the **RAM** . Program instructions may be stored in the EPROM in a number of overlays, and individual overlays selected by either the **bootstrap** program or instructions contained in another overlap overlay may be selectively loaded into the **RAM** for execution. The EPROM is addressed by a programmable counter (60) which appears to the **microprocessor** as an input/output device to be written into.

ADVANTAGE - Low cost, flexible, high access speed. (10pp Dwg.No.3/5)

Title Terms: **MICROPROCESSOR** ; BASED; PROGRAM; STORAGE; **BOOTSTRAP** ; PROGRAM; PROGRAM; INSTRUCTION; STORAGE; EPROM; OVERLAY; INDIVIDUAL; SELECT; **BOOTSTRAP**
Derwent Class: T01
International Patent Class (Additional): G06F-009/06; G06F-012/16
File Segment: EPI

[redacted]

**25/5/1 (Item 1 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


016476302 **Image available**
WPI Acc No: 2004-634245/200461
Related WPI Acc No: 2006-036115
XRPX Acc No: N04-501403
**Remote management sub-system for e.g. server, has management processor that** emulates disk drive **device storing** bootable image **and** boots **managed computer from** image **stored in management memory**
Patent Assignee: BROWN A (BROW-I); HOKE P W (HOKE-I); NEUFELD E D (NEUF-I); PIPKINS J D (PIPK-I)
Inventor: BROWN A; HOKE P W; NEUFELD E D; PIPKINS J D
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week |
|---|---|---|---|---|---|---|
| US 20040162893 | A1 | 20040819 | US 2000675281 | A | 20000929 | 200461 B |
| | | | US 2004781108 | A | 20040218 | |

Priority Applications (No Type Date): US 2000675281 A 20000929; US 2004781108 A 20040218
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 20040162893 | A1 | | 11 | G06F-015/177 | Cont of application US 2000675281 |

Abstract (Basic): US 20040162893 A1

NOVELTY - The system has a bridge logic (165) coupling a management system **bus** (195) to a management processor (155), where the **bus** is configured to couple to an expansion **bus** of a managed computer (100). A management memory (190) coupled to the processor is configured to hold a **bootable image** . The processor **emulates** a **disk drive** device storing the **bootable image** and **boots** the computer from the image stored in the memory.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method for remotely managing a computer system or network.

USE - Used for managing a computer system e.g. server, personal computer, or workstation, or network e.g. LAN.

ADVANTAGE - The management processor **emulates** the **disk drive** device storing the **bootable image** and **boots** the managed computer from the **bootable image** stored in the management memory, thereby allowing the computer to be remotely installed with software even if the computer had failed and could not be booted.

DESCRIPTION OF DRAWING(S) - DESCRIPTION OF DRAWING - The drawing shows a block diagram depicting architecture of a managed computer system, management **card** , and remote management console.

Managed computer (100)
Management processor (155)
Bridge logic (165)
Management memory (190)
Management system **bus** (195)
pp; 11 DwgNo 2/3

Title Terms: REMOTE; MANAGEMENT; SUB; SYSTEM; SERVE; MANAGEMENT; PROCESSOR; DISC; DRIVE; DEVICE; STORAGE; IMAGE; BOOT; COMPUTER; IMAGE; STORAGE; MANAGEMENT; MEMORY
Derwent Class: T01; W01
International Patent Class (Main): G06F-015/177
File Segment: EPI

**30/5/1 (Item 1 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


013911978 **Image available**
WPI Acc No: 2001-396191/200142
XRPX Acc No: N01-291793

**Utility program execution method for computer system, involves directing resource access location to native file system location so that resource subject is accessed despite imposed restrictions**

Patent Assignee: DELL USA LP (DELL-N)
Inventor: OVERFIELD A L; PEARCE J J
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 6192471 | B1 | 20010220 | US 96592504 | A | 19960126 | 200142 | B |

Priority Applications (No Type Date): US 96592504 A 19960126
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 6192471 | B1 | | 23 | G06F-009/00 | |


Abstract (Basic): US 6192471 B1

NOVELTY - A virtual resource reboot command (460) assigning virtual resource in reserved region as a **bootstrap** device, is executed by which interceptor (440) relating a location on the **virtual disk drive** (330) to location in the native film system, is invoked. Access to the virtual resource is intercepted and a resource access location is directed to the native film system location to access resource subject freely.

DETAILED DESCRIPTION - A request performs a utility program that attempts to access the resource in a manner that violates the access restriction. The requested utility program is executed in response to the request by passing the restrictions imposed by the computing environment independent of the particular computing environment. The utility program generates access to the virtual resource. The resource subject is accessed despite the access restrictions imposed by the computing environment. INDEPENDENT CLAIMS are also included for the following:

(a) Computer program;
(b) Computer system

USE - For running computer system in operating environment.

ADVANTAGE - Utility programs have access to all system resources without hindrance from an overlying native operating system. The native operating system and the **virtual drive** are mutually independent and non-interacting so that performance of the active operating system is not influenced by the inactive operating system. The **virtual drive** appears to a computer user simply as a single file. Multiple obscurely named utility files are transparent to the user. The storage resources for implementing the operating environment is removed and installed easily upon user command.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of a system for creating an operating system.

**Virtual disk drive** (330)
Interceptor (440)
Virtual resource reboot command (460)
pp; 23 DwgNo 4/12

Title Terms: UTILISE; PROGRAM; EXECUTE; METHOD; COMPUTER; SYSTEM; DIRECT; RESOURCE; ACCESS; LOCATE; NATIVE; FILE; SYSTEM; LOCATE; SO; RESOURCE; SUBJECT; ACCESS; IMPOSE; RESTRICT

[redacted]

Derwent Class: T01
International Patent Class (Main): G06F-009/00
File Segment: EPI

US006658563B1

(12) **United States Patent**
**Ice, Jr. et al.**

(10) **Patent No.: US 6,658,563 B1**
(45) **Date of Patent: Dec. 2, 2003**

(54) **VIRTUAL FLOPPY DISKETTE IMAGE WITHIN A PRIMARY PARTITION IN A HARD DISK DRIVE AND METHOD FOR BOOTING SYSTEM WITH VIRTUAL DISKETTE**

(75) Inventors: **Herbert Jackson Ice, Jr.**, Austin, TX (US); **Robert Duane Johnson**, Raleigh, NC (US); **Kofi Kekessie**, Durham, NC (US); **David Rhoades**, Apex, NC (US); **Gary Anthony Vaiskauckas**, Morrisville, NC (US)

(73) Assignee: **International Business Machines Corporation**, Armonk, NY (US)

( * ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/574,729**

(22) Filed: **May 18, 2000**

(51) **Int. Cl.**[7] ..... **G06F 15/177**; G06F 1/24
(52) **U.S. Cl.** ..... **713/2**; 713/1; 713/100
(58) **Field of Search** ..... 713/1, 2, 100; 711/173; 700/5

(56) **References Cited**

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"Enhancing Applications Performance on Intel Paragon through Dynamic Memory Allocation", IEEE, 1994, pp. 232–239.*

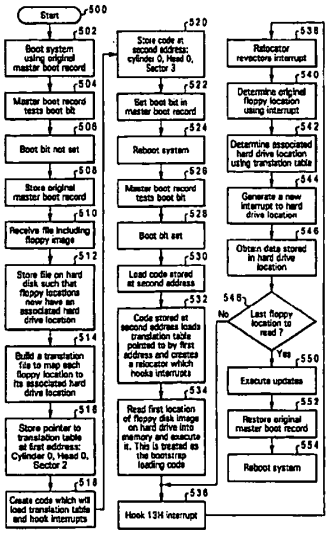
* cited by examiner

*Primary Examiner*—Thomas M. Heckler
*Assistant Examiner*—Chun Cao
(74) *Attorney, Agent, or Firm*—Bracewell & Patterson LLP

(57) **ABSTRACT**

A data processing system and method are described for booting a computer system from a virtual floppy diskette. A native operating system is executed by the computer system which utilizes a native file system. A boot able floppy diskette image is stored on the hard drive. The image includes a second operating system which utilizes a second file system. A master boot record stored on the hard drive is modified to include a boot bit. The boot bit is set in response to a storage of the image. The computer system is then booted from the image in response to the boot bit being set. The native operating system and the native file system are unchanged during the booting of the computer system from the image.

**21 Claims, 4 Drawing Sheets**



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File   6:NTIS 1964-2006/Mar W3
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File  23:CSA Technology Research Database 1963-2006/Mar
         (c) 2006 CSA.
File  34:SciSearch(R) Cited Ref Sci 1990-2006/Mar W3
         (c) 2006 Inst for Sci Info
File  35:Dissertation Abs Online 1861-2006/Mar
         (c) 2006 ProQuest Info&Learning
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         (c)2006 Japan Science and Tech Corp(JST)
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File  99:Wilson Appl. Sci & Tech Abs 1983-2006/Feb
         (c) 2006 The HW Wilson Co.
File 111:TGG Natl.Newspaper Index(SM) 1979-2006/Mar 23
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File 144:Pascal 1973-2006/Mar W1
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File 239:Mathsci 1940-2006/May
         (c) 2006 American Mathematical Society
File 256:TecInfoSource 82-2006/Apr
         (c) 2006 Info.Sources Inc
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info

Set     Items   Description
S1    6795130   HOST? ? OR COMPUTER? ? OR PC? ? OR CLIENT? ?
S2    3624300   DEVICE? ? OR APPARATUS OR SUBSYSTEM? ? OR INTERMEDIAR???
S3     348886   CARD? ? OR BUS OR BUSES OR BUSSES OR NIC
S4       1832   (VIRTUAL OR EMULAT???)(3N)(DISK? ? OR DISKETTE? ? OR DRIVE?
                 ? OR FLOPPY OR FLOPPIES)
S5     181601   S2:S4(3N)(WITHIN OR WITH()IN OR INSIDE OR INTERNAL?? OR EM-
                BED???? OR CONTAIN??? OR INCLUD??? OR COUPLE OR COUPLED OR CO-
                NNECT???)
S6      35979   BOOT????(3N)IMAG??? OR (PREBOOT OR PRE()BOOT)()EXECUT???()-
                ENVIRONMENT OR PXE OR BOOTSTRAP???? OR PREBOOT????
S7     808396   RAM OR MEMORY OR MEMORIES
S8          3   S1 AND S5 AND S6 AND S7
S9          3   RD  (unique items)
S10       130   S3:S4 AND S6
S11         1   S3 AND S4 AND S6
S12        17   S10 AND S7
S13        16   RD  (unique items)
S14        15   S13 NOT S9
S15        13   S14 NOT PY=2001:2006
S16         0   S10 AND CLIENT(3N)MANAG?
S17        24   S10 AND (PROCESSOR? ? OR MICROPROCESSOR? ? OR CPU OR CHIP?
                  ?)
S18        22   RD  (unique items)
S19        10   S18 NOT (S9 OR S14)
S20         9   S19 NOT PY=2001:2006
S21         4   S10 AND REMOT???
S22         3   RD  (unique items)
S23         5   S4 AND S6
S24         4   RD  (unique items)
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S25 3 S23 NOT (S9 OR S14 OR S19 OR S22)
? logoff hold
31mar06 11:55:17 User259273 Session D366.11

**9/5/3 (Item 1 from file: 6)**
DIALOG(R)File 6:NTIS


1111967 NTIS Accession Number: AD-D010 994/2
**Programmable** Bootstrap **Loading System**
(Patent)
Page, R. E. ; Brackett, R. B.
Department of the Navy, Washington, DC.
Corp. Source Codes: 001840000; 110050
Report No.: PAT-APPL-6-113 875; PATENT-4 430 704
Filed 21 Jan 80 patented 7 Feb 84 12p
Languages: English Document Type: Patent
Journal Announcement: GRAI8416
Supersedes PAT-APPL-6-113 875, AD-D006 931.
This Government-owned invention available for U.S. licensing and, possibly, for foreign licensing. Copy of patent available Commissioner of Patents, Washington, DC 20231 $1.00.
NTIS Prices: Not available NTIS
Country of Publication: United States
This report describes a programmable **bootstrap** loader device for loading or transferring programs into the main **memory** of a **computer** system. This **device includes** a processor-peripheral interface for decoding instructions of the **computer** system and for generating control signals to operate peripheral equipment coupled to the system. An alterable or programmable **memory** stores a set of instructions which makes up a **bootstrap** loader program, is not lost when power to the system is shut off. An alterable **memory** access circuit is coupled between the processor-peripheral interface and the alterable **memory** to enable an operator to alter discreet instructions of the stored **bootstrap** loader program. (Author)
Descriptors: *Patents; *Data processing equipment; *Input; * **Computer** programming; Loaders; Transfer; Data storage systems; Instructions; Nonvolatile **memories** ; Decoding; Diagrams
Identifiers: PAT-CL-364-200; NTISGPN
Section Headings: 90F (Government Inventions For Licensing--Electrotechnology); 62A (Computers, Control, and Information Theory--Computer Hardware)

**15/5/4 (Item 4 from file: 2)**
DIALOG(R)File 2:INSPEC


05887036 INSPEC Abstract Number: C9504-6130S-024
**Title: BITS: a smartcard protected operating system**
Author(s): Clark, P.C.; Hoffman, L.J.
Author Affiliation: Trusted Inf. Syst. Inc., Glenwood, MD, USA
Journal: Communications of the ACM vol.37, no.11 p.66-70, 94
Publication Date: Nov. 1994 Country of Publication: USA
CODEN: CACMA2 ISSN: 0001-0782
U.S. Copyright Clearance Center Code: 0001-0782/94/01100$3.50
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: Secure processors as a technology offer a great deal for applications that require enhanced computer security. In general, these processors contain not only computational capability, but **memory** capacity as well. This self-containment makes secure processors resistant to attack, as they need not depend upon potentially vulnerable external resources. The Boot Integrity Token System (BITS) is being developed to provide computer boot integrity and enforce access control. The basic idea behind BITS is that the host computer should actually boot from a smartcard. Since the smartcard can be readily configured to require user authentication prior to data access, it provides an ideal mechanism to secure a host computer. The security of the system assumes the physical security of the host with either a tamper-proof or tamper-evident casing, and the security of the smartcard by its design and configuration. (17 Refs)
Subfile: C
Descriptors: authorisation; computer **bootstrapping** ; data integrity; EPROM; operating systems (computers); smart **cards**
Identifiers: BITS; smartcard protected operating system; secure processors; enhanced computer security; computational capability; **memory** capacity; self-containment; attack resistance; Boot Integrity Token System; access control; user authentication; physical security; tamper-proof casing ; tamper-evident casing
Class Codes: C6130S (Data security); C6150J (Operating systems); C5320G ( Semiconductor storage)

**22/5/3 (Item 1 from file: 256)**
DIALOG(R)File 256:TecInfoSource


00141704 DOCUMENT TYPE: Review

**PRODUCT NAMES: Deployment Solution (133191); Norton Ghost 7.5 (668302); PowerQuest DeployCenter Library 5.01 (133205)**

**TITLE: Disk Imaging Gets a Makeover**
AUTHOR: Robinson, Cornell W, III
SOURCE: Network Computing, v13 n20 p59(9) Sep 30, 2002
ISSN: 1046-4468
HOMEPAGE: http://www.NetworkComputing.com

RECORD TYPE: Review
REVIEW TYPE: Review
GRADE: B

Altiris's Altiris Deployment Solution, Symantec's Norton Ghost 7.5, Microsoft **Remote** Installation Service (RIS), and PowerQuest's PowerQuest Deploy Center 5.01 are reviewed disk imaging solutions. The products streamline and simplify tasks to save time and money and also provide more control over users' workstations. Most IT departments now clone users' PCs over a LAN, a technique that, based on the results of testing, leverages a network-based distribution model to considerably speed disk imaging and eliminate sneaker-net. Intel's Wired for Management **PXE** (Pre-Execution Environment), a standard-based technology, should be on all network interface **cards** and PCs. with **PXE** , client machines boot using the **NIC** , connect, and execute programs stored on a server. With these abilities and Dynamic Host Configuration Protocol Server (DHCP) and TFTP, IT personnel can sit at their desks to update all the software images on the network. Another advantage of disk imaging is network-based image distribution, but a modern network architecture is required in which switches support multicasting, which is supported by all the products except Microsoft RIS. Altiris, the editors' choice, is the easiest to use product and also has the fastest performance. All the other products are lower-priced, and all get similar ratings for ease of use.

COMPANY NAME: Altiris (646784); Symantec Corp (386251)
SPECIAL FEATURE: Tables Screen Layouts
DESCRIPTORS: Configuration Management; Disk Backup; Electronic Software Distribution; LANs; Network Administration; Network Software
REVISION DATE: 20040330

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March 31, 2006 USPTO

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